

#### Abstract of the Disclosure

A necessary number of initial stage element circuits (2), intermediate stage element circuits (1), and final stage element circuits (3) are connected in cascade and combined in parallel arrangement simultaneously. The partial sum output data (8) on the element circuits is synchronized with the inner partial sum data. In this way, it is possible to configure a high-speed high-order and high-precision FIR filter, i.e., a large-scale digital filter. Thus, it is possible to manufacture a high-order and high-precision FIR filter capable of high-speed operation of 2 GHz or above at a low cost.